Intel® 810 Embedded Client Reference Design — Hublink System Partitioning

Scalable Platform with Integrated Flat Panel Display

Application Note

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Contents

Figures

Table

Revision History

Date	Revision	Description
Month Year	001	Initial release of document.

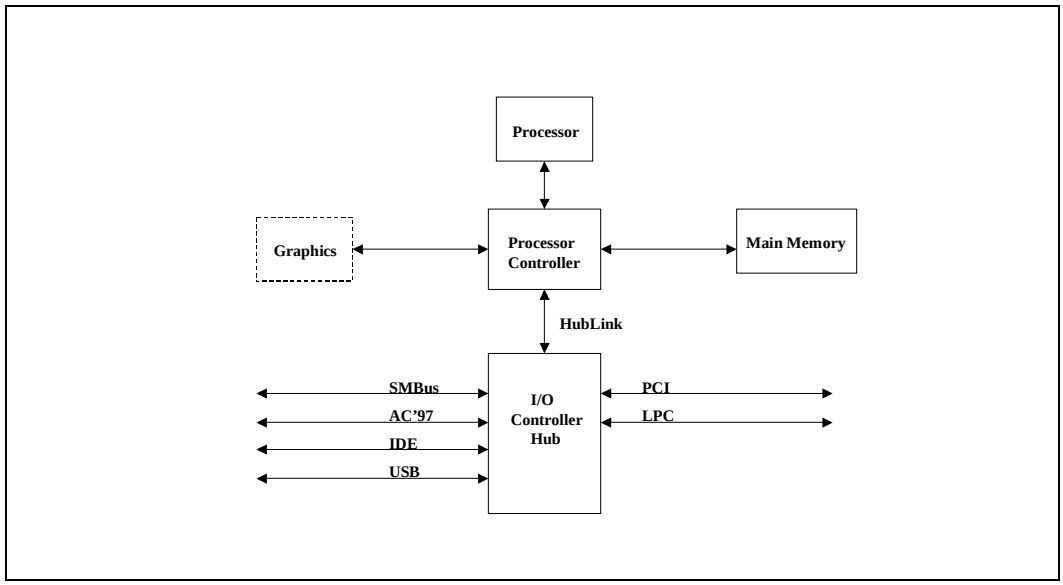
1.0 Introduction

This application note discusses the system partitioning used on the Intel® Embedded Client Reference Design, a transaction terminal proof of concept, to enable a compact versatile system footprint. This paper should not to be used as a typical Intel design guide, but as an application note as to how Intel's 800 series chipsets naturally lend themselves to a system partitioning that can be used in compact embedded applications.

2.0 Intel 800 Series Chipset Architecture

Figure 1 depicts a typical 800 Series Chipset based system.

Figure 1. 800 Series Chipset Architecture



The design of a small footprint, single board system; can lead to extreme difficulties during board layout due to minimum trace length requirements between key components. From looking at the figure above, splitting the system at the HubLink boundary into two boards is the obvious choice for minimizing the system footprint.

This partition is ideal from the standpoint that it minimizes the number of signals that must cross board boundaries, and the interrupted signals have only one source/destination, thereby preventing stubs that could lead to signal integrity difficulties.

3.0 Advantages Of a Two Board System

- Smaller system footprint.
- Natural system partition facilitates the coordination of multiple design resources, enabling quicker design cycles.
- Mixing and matching of boards to satisfy the requirements of multiple applications.

Two separate applications may have similar processing requirements, but vastly different I/O requirements, or vice versa. For example, while two separate applications may have similar processor/memory requirements which could be met by and 82810 GMCH coupled to a 300 MHz Celeron processor, one may require twelve serial ports while the second application may require four USB ports.

A single processor module could be developed that is common to both applications. And two separate I/O modules could be developed to satisfy the unique requirements of each application. Hence, the risky design portion of the processor module needs to be done only once for two different projects, maximizing design reuse and minimizing design risk.

If for some reason, the processing requirements of an existing application change over time, a new processing module could be designed while completely reusing the existing I/O section. An OEM that is constantly designing for new applications, could begin to accumulate a library of processing modules and I/O modules which could be mixed and matched to satisfy the requirements of new unplanned projects.

4.0 Disadvantages Of A Two Board System

- Total system cost is increased slightly due to having to manufacture and assemble two boards versus a single larger board.
- Connectors and fastening hardware is required to join the two boards.
- Most CAD tools do not easily coordinate across multiple boards. The CAD engineer must manually track the length of traces that cross board boundaries.

5.0 Special Considerations for the Connector Between Boards

While Intel's HubLink is a proprietary bus, and specifications are not released to customers, this system partition has been successfully tested on various designs using AMP's Mictor family of connectors. Standard Intel design guides have been followed while laying out boards using these connectors, accounting for the effective length that the connectors add. Mictors are designed to be 50 Ω matched impedance connectors, and are available in various stacking heights and number of circuits. There are two types of contacts: standard gold plating and palladium-nickel plating. The palladium-nickel plating is recommended for applications requiring several mating cycles.

Mictor contacts are very fine and cannot handle much error in misalignment. The design of the processing block and I/O block need to consider the manufacturing error of the boards as well as the errors caused by the reflow process. If a single connector joins the boards, then the connectors will be free to align themselves only if there are no other fasteners preventing the two boards from moving slightly relative to one another. Applications that require more than one connector between boards must consider all tolerances to ensure alignment and a reliable contact. See AMP's Application Specification #114-11004 for further information regarding the use and assembly of Mictor connectors.

6.0 Connector Signal Assignment

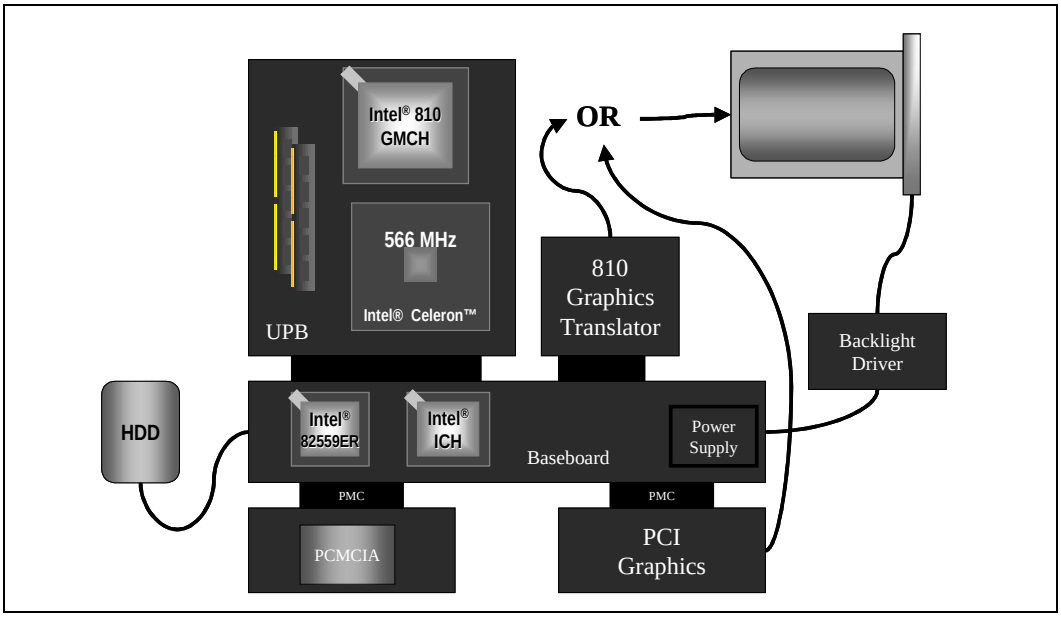
Consideration needs to be given when making signal assignments to the connector. For example, Intel design guides specify matched lengths for the HubLink lines as well as routing the HubLink strobe lines as a differential pair, and separation of HubLink signals from other signals. Connector signal assignments must be made so as to comply with Intel design guides. Please follow the routing guidelines published in the Intel® 810 Chipset Design Guide (order number 290657).

The HubLink signals and clock signals are the most sensitive signals. They should be assigned so as to be away from other signals and adjacent to ground pins. As always, adequate power and ground pins need to be allocated to ensure clean power distribution.

7.0 Intel® Embedded Client Reference Design Architecture

The figure below represents the Intel® Embedded Client Reference Design Interconnect Diagram. The Universal Processing Block (UPB) and Baseboard (BB) comprise the main system.

Figure 2. Interconnect Diagram



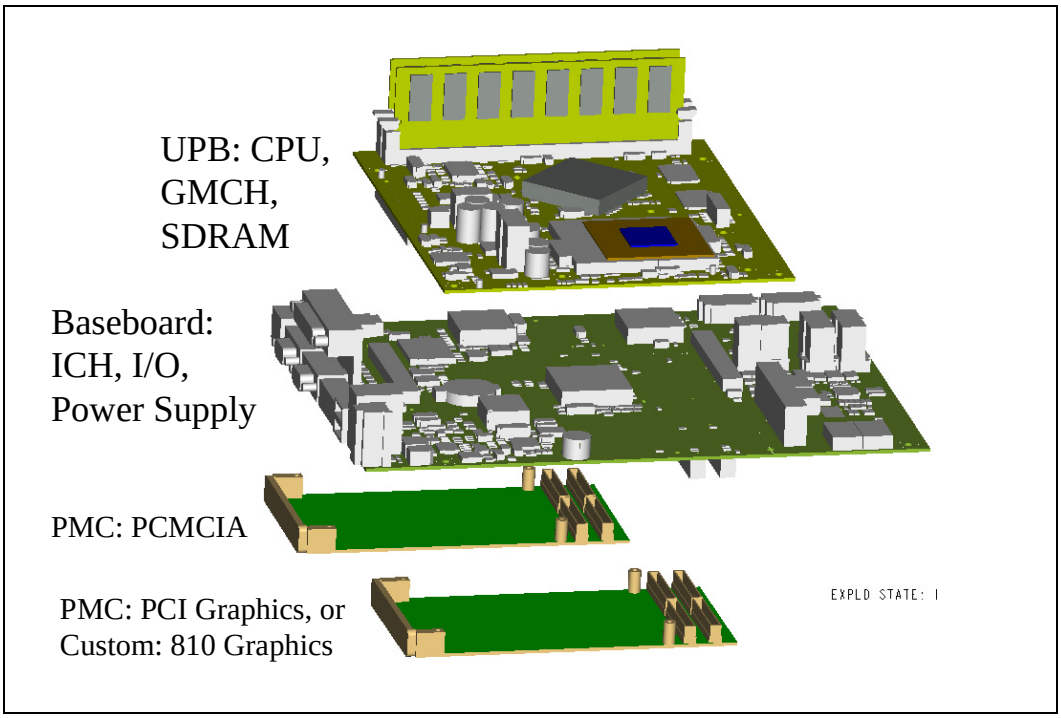
The processor, GMCH, and several other critical circuits reside on the UPB. The CPU core supply was placed near the processor to more easily satisfy the transient supply requirements of the CPU. The memory DIMMs were located near the GMCH to ease routing constraints and minimize the number of circuits required of the Mictor connector. The clock driver was placed on the UPB due to the majority of high frequency clock signals being required by the CPU, GMCH and DIMMs.

All of the system I/O was located on the BB. The intent was to make the UPB entirely independent of I/O and not encumber other applications with the I/O requirements of Bloomington. Therefore, all of the reference design's I/O requirements were placed on the BB.

8.0 Bloomington Mechanical Depiction

The picture below illustrates the physical realization of this design for the Intel Embedded Client Reference Design. It was not designed to meet the cost requirements of a high volume application, but as a versatile proof of concept. For example; the 810 Graphics Translator board, the PCMCIA module, and the PCI Graphics module could all be integrated onto the baseboard for a lower total system cost.

Figure 3. System Boards



9.0 Vendor List

Table 1 provides a vendor list as a service to our customers for reference only. The inclusion of this list should not be considered a recommendation or product endorsement by Intel Corporation.

Table 1. Vendor List

Product Type: High Speed Connectors
AMP/Mictor http://catalog.tycoelectronics.com/AMP/bin/AMP.Connect?M=CINF&C=11473&N=1&RQS=C~11473^M~FEAT
Product Type: Power Control Circuits
Linear Technology (http://www.linear-tech.com/)
Analog Devices (http://www.analog.com/)
Product Type: Capacitors
United Chemi-Con (http://www.chemi-con.com/)
AVX (http://www.avxcorp.com/products/capacitors)
Product Type: Inductors
Central Technologies (http://www.ctparts.com/)
Coilcraft (http://www.coilcraft.com/)
Coiltronics (http://www.coiltronics.com/)
Product Type: FETs
Siliconix (http://www.siliconix.com/)
Fairchild (http://www.fairchildsemi.com/)